Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading of an instruction in the code into a cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction, wherein the metadata comprises a prefetch indicator that is associated with the instruction by one of being placed in the instruction [[or]] and stored in a shadow memory;

responsive to a determination of the metadata being present for the instruction, determining whether data is to be prefetched, wherein the step of determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a first threshold value, and determining whether a number of cache lines chosen to be replaced is greater than a second threshold value; and

responsive to a determination that data is to be prefetched, prefetching data, from within a data structure using the metadata, into the cache in the processor, wherein the step of prefetching comprises one of prefetching the data responsive to determining that the number of outstanding cache misses is less than the first threshold value, and prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the second threshold value.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The method of claim 1, wherein the prefetching step includes: retrieving the data from within the data structure using a pointer and an offset value.

5. (Previously Presented) The method of claim 1, wherein the prefetching step includes: retrieving the data from the data structure using an address.

6. (Currently Amended) The method of claim 1, wherein the processor unit is selected from one of an instruction cache [[or]] and a load/store unit.

7. (Original) The method of claim 1, wherein the cache is an instruction cache.

8. (Original) The method of claim 4, wherein the metadata includes the pointer and the offset value.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Currently Amended) A data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the data processing system comprising:

first determining means, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present for the instruction, wherein the metadata comprises a prefetch indicator associated with the instruction by one of being placed in the instruction [[or]] and stored in a shadow memory;

second determining means, responsive to a determination of the metadata being present for the instruction, for determining whether data is to be prefetched, wherein the second determining means comprises one of means for determining whether a number of outstanding cache misses is less than a first threshold value, and means for determining whether a number of cache lines chosen to be replaced is greater than a second threshold value; and

prefetching means, responsive to a determination that data is to be prefetched, for prefetching data, from within a data structure using the metadata, into the cache in the processor, wherein the prefetching means comprises one of means for prefetching the data when it is determined that the number of outstanding cache misses is less than the first threshold value, and means for prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the second threshold value.

13. (Canceled)

14. (Canceled)

15. (Previously Presented) The data processing system of claim 12, wherein the prefetching means includes:

retrieving means for retrieving the data from within the data structure using a pointer and an offset value.

16. (Previously Presented) The data processing system of claim 12, wherein the prefetching means includes:

retrieving means for retrieving the data from the data structure using an address.

17. (Currently Amended) The data processing system of claim 12, wherein the processor unit is selected from one of an instruction cache [[or]] and a load/store unit.

18. (Currently Amended) A computer program product in a recordable-type computer readable medium for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the computer program product comprising:

first instructions, responsive to loading of an instruction in the code into a cache, for determining, by a processor unit, whether metadata for a prefetch is present for the instruction, wherein the metadata comprises a prefetch indicator associated with the instruction by one of being placed in the instruction [[or]] and stored in a shadow memory;

second instructions, responsive to a determination of the metadata being present for the instruction, for determining whether data is to be prefetched, wherein the second instructions comprises one of instructions for determining whether a number of outstanding cache misses is less than a first threshold value and instructions for determining whether a number of cache lines chosen to be replaced is greater than a second threshold value; and

responsive to a determination that data is to be prefetched, third instructions for prefetching data, from within a data structure using the metadata, into the cache in the processor, wherein the third instructions comprises one of instructions for prefetching the data when it is determined that the number of outstanding cache misses is less than the first threshold value, and instructions for prefetching the data when it is determined that the number of cache lines chosen to be replaced is greater than the second threshold value.

19. (Canceled)

20. (Canceled)

21. (Previously Presented) The computer program product of claim 18, wherein the third instructions includes:

sub-instructions for retrieving the data from within the data structure using a pointer and an offset value.

22. (Previously Presented) The computer program product of claim 18, wherein the third instructions includes:

sub-instructions for retrieving the data from the data structure using an address.

23. (Currently Amended) The computer program product of claim 18, wherein the processor unit is selected from one of an instruction cache [[or]] and a load/store unit.

24. (Currently Amended) A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:

responsive to loading of an instruction in the code into an instruction cache, determining, by a processor unit, whether metadata for a prefetch is present for the instruction, wherein the processor unit comprises one of the instruction cache [[or]] and a load/store unit, and wherein the metadata comprises a prefetch indicator associated with the instruction by one of being placed in the instruction [[or]] and stored in a shadow memory, and comprises a pointer and an offset value;

responsive to a determination of the metadata being present for the instruction, determining whether data is to be prefetched, wherein the step of determining whether data is to be prefetched comprises one of determining whether a number of outstanding cache misses is less than a first threshold value, and determining whether a number of cache lines chosen to be replaced is greater than a second threshold value; and

responsive to a determination that data is to be prefetched, prefetching data, from within a data structure into the instruction cache in the processor using the pointer and the offset value, wherein the step of prefetching comprises one of: prefetching the data responsive to determining that the number of outstanding cache misses is less than the first threshold value, and prefetching the data responsive to determining that the number of cache lines chosen to be replaced is greater than the second threshold value.